WE CLAIM:

1. A field effect device, comprising:

a crystalline Si body of one conductivity type;

a SiGe layer epitaxially disposed on said Si body;

a Si layer epitaxially disposed on said SiGe layer; and

a source and a drain comprising SiGe in an epitaxial relation with the Si body and connected to each other by the SiGe layer and the Si layer, the source and the drain having a conductivity type opposite to that of the Si body and each forming a heterojunction and a metallurgical junction with the Si body, wherein the heterojunction coincides with the metallurgical junction with a tolerance of less than about 10nm.

2. The device of claim 1, wherein the tolerance is less than about 5nm.

3. The device of claim 1, wherein the Si body is disposed on top of an insulating layer.

4. The device of claim 3, wherein the insulating layer is SiO_2.

5. The device of claim 1, wherein the Si body conductivity is n-type, and wherein a hole device current is confined predominantly in the SiGe layer.

6. The device of claim 5, wherein the hole device current is directed along one of a <100> or a <110> crystallographic direction.

7. The device of claim 1, wherein the Si body conductivity is p-type, and an electron device current is confined predominantly in the Si layer.

8. The device of claim 1, wherein the SiGe layer and the SiGe in the source and the drain are compressively strained.

9. The device of claim 1, wherein the SiGe layer is between about 5nm and 15nm thick.

10. The device of claim 1, wherein the SiGe layer has a Ge concentration which substantially equals a Ge concentration in the SiGe in the source and the drain.

11. The device of claim 10, wherein the Ge concentration in the SiGe layer is between about 15% and 50%.

12. The device of claim 1, wherein the device has a top surface plane, and wherein the source and the drain are raising above the top surface plane.

13. The device of claim 1, wherein the device has a top surface plane that lies essentially in one of a (100), (110) or (111) crystallographic plane.

14. The device of claim 1, wherein the source and the drain further comprise an epitaxial Si cap layer disposed on top of the strained SiGe, wherein the Si cap layer is between about 2nm and 30nm thick.

15. The device of claim 1, wherein the Si body conductivity is n-type, and the device is connected in a complementary circuit configuration with a field effect device comprising:

a crystalline Si body of p-type conductivity;

a SiGe layer epitaxially disposed on the p-type Si body;

a Si layer epitaxially disposed on the SiGe layer; and

a source and a drain of n-type conductivity comprising SiGe in an epitaxial relation with the p-type Si body and connected to each other by the SiGe layer and the Si layer, the source and the drain each forming a heterojunction and a metallurgical junction with the p-type Si body, wherein the heterojunction coincides with the metallurgical junction with a tolerance of less than about 10nm.

16. The device of claim 1, wherein the Si body conductivity is n-type, and the device is connected in a complementary circuit configuration with a field effect device comprising:

a crystalline Si body of p-type conductivity;

a SiGe layer epitaxially disposed on the p-type Si body;

a Si layer epitaxially disposed on the SiGe layer; and

a source and a drain of n-type conductivity comprising SiGe in an epitaxial relation with the p-type Si body and connected to each other by the SiGe layer and the Si layer.

17. The device of claim 1, wherein the Si body conductivity is n-type, and the device is connected in a complementary circuit configuration with a field effect device comprising:

a crystalline Si body of p-type conductivity;

a SiGe layer epitaxially disposed on the p-type Si body;

a Si layer epitaxially disposed on the SiGe layer; and

a source and a drain of n-type conductivity connected to each other by the SiGe layer and the Si layer.

18. The device of claim 1, wherein the Si body conductivity is n-type, and the device is connected in a complementary circuit configuration with an NMOS device.

19. A PMOS field effect device, comprising:

a crystalline Si body of n-type conductivity;

a SiGe layer epitaxially disposed on the n-type Si body;

a Si layer epitaxially disposed on the SiGe layer; and

a source and a drain of p-type conductivity comprising SiGe in an epitaxial relation with the n-type Si body and connected to each other by the SiGe layer and the Si layer, the source and the drain each forming a heterojunction and a metallurgical junction with the n-type Si body, wherein the heterojunction coincides with the metallurgical junction with a tolerance of less than about 10nm.

20. The device of claim 19, wherein the tolerance is less than about 5nm.

21. The device of claim 19, wherein the Si body is disposed on top of an insulating layer.

22. The device of claim 21, wherein the insulating layer is SiO_2.

23. The device of claim 19, wherein the SiGe layer is between about 5nm and 15nm thick.

24. The device of claim 19, wherein the SiGe layer has a Ge concentration of between about 15% and 50%.

25. The device of claim 24, wherein the Ge concentration in SiGe layer substantially equals a Ge concentration in the SiGe in the source and the drain.

26. A method for producing a field effect device comprising the step of:

fabricating a source and a drain by epitaxial deposition of a first material, wherein the first material forms a heterojunction with a second material, and wherein the second material constitutes a body of the device.

27. The method of claim 26, further comprising the step of:

providing a channel between the source and the drain, wherein the channel consists essentially of the first material.

28. The method of claim 26, further comprising the step of:

providing a channel between the source and the drain, wherein the channel consists essentially of the second material.

29. The method of claim 26, further comprising the step of:

providing the body with one conductivity type and providing the source and the drain with an opposing conductivity type forming a metallurgical junction between the body and the source and the drain, and wherein the heterojunction and the metallurgical junction coincide with a tolerance of less than about 10nm.

30. The method of claim 29, wherein the body conductivity is selected one of n-type or p-type.

31. The method of claim 27, wherein the first material is selected to be SiGe and the second material is selected to be Si.

32. The method of claim 31, wherein the body is selected to be a Si layer on an insulator.

33. The method of claim 31, wherein in the epitaxial deposition the SiGe is selected to be in one of an undoped state or a p-doped state.

34. The method of claim 31, wherein in the epitaxial deposition the SiGe is selected to have a Ge concentration of between about 15% and 50%.

35. The method of claim 31, wherein the SiGe channel is selected to be between about 5nm and 15nm thick.

36. The method of claim 26, further comprising the step of capping the first material with an epitaxial layer of the second material having a thickness of between about 2nm and 30nm.

37. The method of claim 26, wherein the device has a top surface plane and the source and the drain are fabricated to raise above the top surface plane.

38. A processor, comprising:

at least one chip, wherein the chip comprises at least one field effect device, and wherein the at least one field effect device comprise:

a crystalline Si body of one conductivity type;

a SiGe layer epitaxially disposed on the Si body;

a Si layer epitaxially disposed on the SiGe layer; and

a source and a drain comprising SiGe in an epitaxial relation with the Si body and connected to each other by the SiGe layer and the Si layer, the source and the drain having a conductivity type opposite to that of the Si body and each forming a heterojunction and a metallurgical junction with the Si body, wherein the heterojunction coincides with the metallurgical junction with a tolerance of less than about 10nm.